

Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) ~~Pipeline-synchronisation~~ A pipeline synchronization device for transferring data between clocked devices (~~WD, RD~~) having different clock frequencies (~~CLK~~), comprising:

a mousetrap buffer (~~MT, MT1, MT2~~) for exchanging data (~~Wdat, Rdat~~) with one of ~~said external~~ the clocked devices (~~WD, RD~~), ~~said the~~ mousetrap buffer (~~MT, MT1, MT2~~) ~~having~~ including a signalling output (~~Wack, Rreq~~) for coordinating the data exchange with the ~~external~~ clocked device (~~WD, RD~~), and characterised by a ~~synchroniser (S1, S2)~~ synchronizer that is configured to ~~synchronising the change~~ synchronize a change in a ~~the~~ signalling output (~~Wack, Rreq~~) with the a clock (~~CLK~~) of the ~~external~~ clocked device (~~WD, RD~~).

2. (Currently amended) ~~Pipeline-synchronisation device according to~~ The device of claim 1, wherein the ~~synchroniser (S1)~~ synchronizer is ~~adapted~~ configured to ~~synchronising~~ synchronize the change in the signalling output (~~Wack, Rreq~~) with a high phase or a low phase of the clock (~~CLK~~) of the external device (~~WD, RD~~).

3. (Currently amended) ~~Pipeline-synchronisation device according to~~ The device of claim 2, wherein the ~~synchroniser (S1)~~ synchronizer is ~~adapted~~ configured to delaying a transfer of a ~~the~~ change in the signalling output (~~Wack, Rreq~~) until the clock (~~CLK~~) of the ~~external~~ clocked device (~~WD, RD~~) is ~~either high or low~~ in a given state.

4. (Currently amended) ~~Pipeline synchronisation device according to~~ The device of claim 3, wherein the ~~synchroniser (S1) comprises a synchronising~~ synchronizer ~~includes a synchronizing latch (L) having that includes: a synchronising~~ synchronizing input-(SI) for receiving the signalling output-(Wack, Rreq), a ~~synchronising~~ synchronizing output-(SO) for outputting the received signalling output-(Wack, Rreq) to the ~~external clocked device (WD, RD)~~ and a control input-(e) for enabling the output of the received signalling output-(Wack, Rreq) to the ~~external clocked device (WD, RD)~~.

5. (Currently amended) ~~Pipeline synchronisation device according to~~ The device of claim 4, wherein the ~~synchroniser (S1) comprises~~ synchronizer ~~includes~~ an EXNOR-gate-(50) having two inputs and one output, the inputs of the EXNOR-gate-(50) being connected to the ~~synchronising~~ synchronizing input-(SI) and output-(SO) of the ~~synchronising~~ synchronizing latch-(L), and the ~~synchroniser (S1) comprises~~ synchronizer ~~includes~~ a wait-component-(Wait4) having an input-(d) connected to the output of the EXNOR-gate-(50), an input connected to the clock-(CLK) of the ~~external clocked device (WD, RD)~~ and an output connected to the control input-(e) of the ~~synchronising~~ synchronizing latch-(L).

6. (Currently amended) ~~Pipeline synchronisation device according to~~ The device of claim 5, wherein the wait-component-(Wait4) is ~~adapted~~ configured to outputting signal a change from low to high ~~in-of~~ the input-(d) ~~only~~, if the clock-(CLK) of the ~~external clocked device (WD, RD)~~ is ~~high in a given state~~, and ~~outputting to signal~~ a change from high to low ~~in-of~~ the input-(d) irrespective of the state of the clock-(CLK) of the ~~external clocked device (WD, RD)~~.

7. (Currently amended) ~~Pipeline synchronisation device according to~~ The device of claim 6, wherein the wait-component-(Wait4) comprises an inverter-(65) and an arbiter-(60) having an input for receiving the ~~an~~ inverted clock signal-(CLK), which is ~~inverted by~~ from the inverter-(65), and an input-(d) for receiving the output of the EXNOR-gate-(50) and an output for transmitting the input-(d).

8. (Currently amended) ~~Pipeline-synchronisation device according to~~ The device of claim 1, wherein the ~~synchroniser (S2)~~ synchronizer is adapted configured to ~~synchronising~~ synchronize the change in the signalling output (~~Wack, Rreq~~) with a rising and/or a falling edge of the clock (~~CLK~~) of the ~~external clocked device (WD, RD)~~.

9. (Currently amended) ~~Pipeline-synchronisation device according to~~ The device of claim 8, wherein the ~~synchroniser (S2)~~ synchronizer includes two ~~synchroniser (S1) according to claim 3, which are adapted~~ synchronizers that are configured to delaying a transfer of a change in the signalling output (~~Wack, Rreq~~) until the clock (~~CLK~~) of the ~~external clocked device (WD, RD)~~ is either high or low in a given state, wherein a first of the two ~~synchronisers (S1) is adapted~~ synchronizers is configured to transferring a change in the signalling output (~~Wack, Rreq~~) of a first mousetrap buffer (~~MT1~~) to the ~~external clocked device (WD, RD)~~ and wherein a second of the two ~~synchronisers (S1)~~ synchronizers receives an inverted clock (~~CLK~~) of the ~~external clocked device (WD, RD)~~ and is adapted configured to transferring the a signalling output of a second mousetrap buffer (~~MT2~~) to the first mousetrap buffer (~~MT1~~).

10. (Currently amended) ~~Pipeline-synchronisation device according to~~ The device of claim 8, wherein the ~~synchroniser (S2)~~ synchronizer includes an edge ~~synchroniser (UE4) having~~ synchronizer that includes two wait-components (~~Wait4~~) according to claim 6, each being adapted configured to outputting signal a change from low to high in the input (~~d~~) only, if a received clock is high in a given state, and outputting to signal a change from high to low in the input (~~d~~) irrespective of the state of the received clock, wherein a first of the two wait-components (~~wait4~~) is adapted configured to receiving-receive the clock of the ~~external clocked device (WD, RD)~~ and to signal outputting a change in its input (~~ar~~) to the ~~external clocked device~~, and wherein a second of the two wait components (~~wait4~~) is adapted configured to receiving-receive an inverted clock (~~CLK~~) from the ~~external clocked device (WD, RD)~~

and ~~outputting to signal~~ a change in its input ~~(d)~~ to the input ~~(ar)~~ of the first wait component ~~(wait4)~~.

11. (Currently amended) ~~Pipeline synchronisation device according to~~ The device of claim 10, wherein the synchroniser ~~(S2)~~ comprises synchronizer includes a ~~synchronising~~ synchronizing latch ~~(L)~~ having a ~~synchronising~~ synchronizing input ~~(SI)~~ for receiving the signalling output ~~(Wack, Rreq)~~, a ~~synchronising~~ synchronizing output ~~(SO)~~ for outputting the received signalling output ~~(Wack, Rreq)~~ to the external clocked device ~~(WD, RD)~~ and a control input ~~(e)~~ for enabling the output of the received signalling output ~~(Wack, Rreq)~~ to the external clocked device ~~(WD, RD)~~.

12. (Currently amended) ~~Pipeline synchronisation device according to~~ The device of claim 11, wherein the synchroniser ~~(S2)~~ comprises synchronizer includes an EXNOR-gate ~~(50)~~ having two inputs and one output, the inputs of the EXNOR-gate ~~(50)~~ being connected to the ~~synchronising~~ synchronizing input ~~(SI)~~ and output ~~(SO)~~ of the ~~synchronising~~ synchronizing latch ~~(L)~~, and the synchroniser ~~(S2)~~ comprises synchronizer includes an edge-synchroniser ~~(UE4)~~ synchronizer having an input ~~(d)~~ connected to the output of the EXNOR-gate ~~(50)~~, an input connected to the clock ~~(CLK)~~ of the external clocked device ~~(WD, RD)~~ and an output connected to the control input ~~(e)~~ of the ~~synchronising~~ synchronizing latch ~~(L)~~.

13. (Currently amended) ~~Pipeline synchronisation device according to~~ The device of claim 1, wherein the mousetrap buffer ~~(MT1)~~ is ~~adapted~~ configured to ~~receiving~~ receive data ~~(Wdat)~~ from the external clocked device ~~(WD)~~ and the mousetrap buffer ~~has~~ includes a signalling output ~~(Wack)~~ for acknowledging the receipt of data to the external clocked device ~~(WD)~~.

14. (Currently amended) ~~Pipeline synchronisation device according to~~ The device of claim 1, wherein the mousetrap buffer ~~(MT2)~~ is ~~adapted~~ configured to transferring data ~~(Rdat)~~ to the ~~external~~ clocked device ~~(RD)~~ and the mousetrap buffer has includes a signalling output ~~(Rreq)~~ for requesting the transfer of data to the ~~external~~ clocked device ~~(RD)~~.

15. (Currently amended) ~~Pipeline synchronisation device according to~~ The device of claim 13, wherein the mousetrap buffer ~~(MT1)~~ ~~comprises~~ includes an EXOR-gate for receiving a read request signal ~~(Rreq)~~ from the mousetrap buffer ~~(MT1)~~ and a read acknowledge signal ~~(Rack)~~, a latch ~~(L)~~ having a control input ~~(e)~~ for enabling and disabling the receiving and transferring of data, wherein the ~~synchroniser is adapted~~ synchronizer is configured to ~~synchronising~~ synchronize an output ~~(d)~~ of the EXOR-gate with the clock ~~(CLK)~~ of the ~~external~~ clocked device ~~(WD)~~ and to supply the ~~synchronised output (d)~~ of the EXOR-gate to the control input ~~(e)~~ of the latch ~~(L)~~.

16. (Currently amended) ~~Pipeline synchronisation device according to~~ The device of claim 15, wherein the ~~synchroniser (S2)~~ synchronizer is ~~adapted~~ configured to ~~synchronising the~~ synchronize a change in the output ~~(d)~~ of the EXOR-gate with a rising and/or a falling edge of the clock ~~(CLK)~~ of the ~~external~~ clocked device ~~(WD)~~.

17. (Currently amended) ~~Method~~ A method for transferring data between clocked devices having different clock frequencies ~~(CLK)~~, comprising: ~~the steps of~~
 ~~using a mousetrap buffer for exchanging data (Wdat, Rdat) with one of said~~
 ~~external~~ the clocked devices ~~(WD, RD)~~, wherein said via a mousetrap buffer ~~(MT,~~
 ~~MT1, MT2)~~ outputs that is configured to output a signal ~~(Wack, Rreq)~~ for coordinating
 the data exchange with the ~~external~~ clocked device, and ~~characterised by the step of~~
 ~~synchronising the change~~ synchronizing changes in the output signal ~~(Wack,~~
 ~~Rreq)~~ with the clock ~~(CLK)~~ of the ~~external~~ clocked device ~~(WD, RD)~~.